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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,601	03/20/2001	Tetsuji Kishi	60188-045	9328

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EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 12/03/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,601	KISHI ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *10 and 11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *5* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

1. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 2 recites the limitation "the bus control section". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-9, 12-15, 17-28, 30-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimomura et al. (U.S. Patent No. 6,600,492).

Referring to claims 1, 12, and 25, Shimomura et al. teach a picture processing apparatus comprising, as shown in Fig. 1, a CPU 500 (external unit) for generating an instruction to be executed by the graphic processor 100 on the basis of the program. The generated instruction is then stored in the rendering-data storage area 720 of the memory unit 700 by way of the CPU bus 550, the CPU I/F circuit 310 (receiving unit) and the

internal bus 110 (transferring unit). When a rendering process is started, the graphic processor 100 reads out the instruction, which has been stored in the rendering-data storage area 720 of the memory unit 700 by the CPU 500. The rendering circuit 320 (display data generation section) generates data to be displayed on the liquid-crystal display unit 20000 in accordance with the instruction and stores the data into the memory unit 700. The data stored in the memory unit 700 is then read out by the display circuit 340 (image display section) employed in the graphic processor 100 so as to be displayed on the liquid-crystal display unit 20000. In an operation to display map data as described above, the rendering circuit 320 and the display circuit 340 make accesses to the memory unit 700. At that time, the bus control circuit 200 arbitrates contentions for accesses between the rendering circuit 320 and the display circuit 340 (col. 5, lines 20-42). Shimomura et al. further teach when the CPU I/F circuit 310 receives a request to use the internal bus 110 for making an access to the memory unit 700 from the CPU 500, the CPU I/F circuit 310 issues a request 313 to acquire a bus right to use the internal bus 110 for making an access to the memory unit 700 to the bus control circuit 200 (col. 6, lines 22-27). The rendering circuit 320 reads out a rendering command from the rendering-data storage area 720 to create graphic rendered data and stores the graphic rendered data in the frame buffer 740 (col. 6, lines 48-52).

In regard to claims 2-3, 14-15, 17, 27-28, and 30, Shimomura et al. teach the bus control circuit 200 (Fig. 1) compares the degrees of urgency of accesses to the memory unit 700 to be made by the CPU I/F circuit 310, the rendering circuit 320, the video input circuit 330 and the display circuit 340 by analyzing the internal-state signals 311, 321, 331 and 341 received from the CPU I/F circuit 310, the rendering circuit 320, the video

input circuit 330 or the display circuit 340, respectively, in order to dynamically determines levels of priority to use the internal bus 110 for making an access to the memory unit 700 for the CPU I/F circuit 310, the rendering circuit 320, the video input circuit 330 and the display circuit 340 (col. 8, lines 28-39).

In regard to claims 4-5, and 18-19, Shimomura et al. teach the rendering circuit 320 makes an access to the memory unit 700 by issuing a request 323 for a right to use the internal bus 110 for making an access to the memory unit 700 to the bus control circuit 200 and waiting for an acknowledgment 324 to be output by the bus control circuit 200 in response to the request 323. To put it in detail, first of all, the rendering circuit 320 compares an elapsed time since an internal buffer used as a read buffer became empty and an elapsed time since an buffer used as a write buffer became full, determining which elapsed time is longer. Then, the rendering circuit 320 outputs an internal-state signal 321 representing the longer elapsed time (estimation data processing amount) to the bus control circuit 200. If a result 322 of a judgment on a priority level output by the bus control circuit 200 to the rendering circuit 320 in response to the internal-state signal 321 indicates that the priority level of the rendering circuit 320 to use the internal bus 110 for making an access to the memory unit 700 is highest, the rendering circuit 320 outputs the request 323 to use the internal bus 110 for making an access to the memory unit 700 immediately to the bus control circuit 200 (col. 6, lines 48-67, and col. 7, lines 1-4), and thus, data transfer operation of supplying graphics command from the memory to the display data generation section is higher than the priority of data transfer operation of transferring the graphics command to the memory.

In regard to claims 6-7, 20-21, Shimomura et al. teach when the CPU I/F circuit 310 shown in FIG. 2 receives a request to use the internal bus 110 for making an access to the memory unit 700 from the CPU 500, an elapsed time since the arrival of the access request is measured and an internal-state signal 311 representing the measured elapsed time is output to the bus control circuit 200 (col. 6, lines 22-46). It is implied that the elapsed time is related to the amount of data of graphics commands from the CPU to the memory. As shown in Fig. 6A, Shimomura et al. teach the internal-state signals 311 and 321 generated by the CPU I/F circuit 310 and the rendering circuit 320, respectively, are supplied to the B priority judging circuit 6200 to be compared with each other. As a result of the comparison, the internal-state signal 311 or 321 representing the smaller value is output as a first priority-circuit signal 6201, while the other is output as a second priority-circuit signal 6202 (col. 13, lines 63-67, and col. 14, lines 1-3). Therefore, when the CPU I/F circuit 310 is given the highest priority, which means the internal-state signal 311 (from the CPU I/F) having smaller value than the internal-state value 321 (of the display data generation section), the priority of data transfer operation of transferring graphics command to the memory is higher than the priority of data transfer operation of supplying a graphics command from the memory to the display data generation section.

In regard to claims 8, 22, and 31, as shown in fig. 1, Shimomura et al. teach the CPU interface 310 is connected to an external bus 550, and as cited above, the CPU I/F 310 monitor the amount of data transferring through the elapsed time measured since the arrival of the access request, and the bus control changes the priority based on the amount of data being transferred.

Referring to claims 9 and 23-24, as shown in Fig. 3, Shimomura et al. teach the rendering circuit 320 comprising a command buffer 3200 and a rendering core 3100 (decoding section) for reading out a rendering command from the command buffer 3200. Shimomura et al. further teach if the access is an access to read out a command or texture data from the command buffer 3200 or the texture buffer 3300 respectively, the rendering core 3100 outputs an address (a check address) to the internal bus 110 and then reads out a command or texture data which has been received from the internal bus 110 and stored in the command buffer 3200 or the texture buffer 3300. If the access is an access to write graphical data into the write buffer 3400, on the other hand, the rendering core 3100 outputs an address to the internal bus 110 through the write buffer 3400 and then writes the graphical data into the write buffer 3400 to be eventually output to the internal bus 110 (col. 6, lines 48-67, and col. 7, lines 1-4). It is inherent that the address stored in the buffers should be in a predetermined order.

In regard to claims 13 and 26, as shown in Fig. 1, the CPU, the display data generation section, and the display section share the bus 110.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 16 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimomura et al. (U.S. Patent No. 6,600,492) in view of Meinerth et al. (U.S. Patent No. 5,321,806).

Referring to claims 16 and 29, as cited above, Shimomura et al. teach all the limitations of claims 16 and 29, except for the graphics command including a variable length data.

However, Meinerth et al. teach a method of transferring graphics commands of varying length from the CPU to a memory (col. 2, lines 5-8).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Meinerth et al. in combination with the method as taught by Shimomura et al. so as to give the system designer the freedom to create command set (col. 1, lines 64-67, and col. 2, lines 1-2).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

11/20/2003

Matthew C. Bella

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